Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.119”**

**PAD FUNCTION:**

1. **N.C.**
2. **N.C.**
3. **VCC**
4. **REF OUT (+10V)**
5. **REF GND**
6. **REF IN**
7. **–VEE**
8. **BIPOLAR OFFSET IN**
9. **DAC OUT**
10. **10V SPAN R**
11. **20V SPAN R**
12. **POWER GND**
13. **BIT 12 IN (LSB)**
14. **BIT 11 IN**
15. **BIT 10 IN**
16. **BIT 9 IN**
17. **BIT 8 IN**
18. **BIT 7 IN**
19. **BIT 6 IN**
20. **BIT 5 IN**
21. **BIT 4 IN**
22. **BIT 3 IN**
23. **BIT 2 IN**
24. **BIT 1 IN (MSB)**

**MASK**

**REF**

**ADI**

**E565**

**8**

**7**

**6**

**1**

**5**

**4**

**3**

**14 13 12 12 11 10 9**

**22 23 24**

**15**

**16**

**17**

**18**

**19**

**20**

**21**

**.146”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size = .004” X .004” min.**

**Backside Potential:**

**Mask Ref: E565**

**APPROVED BY: DK DIE SIZE .119” X .146” DATE: 2/28/23**

**MFG: ANALOG DEVICES THICKNESS .019” P/N: AD565A**

**DG 10.1.2**

#### Rev B, 7/1